IN THE DRAWINGS

The attached sheets of drawings include new Figs. 10-19.

Attachment: New Drawing Sheets

REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 17-30 are pending in this application. No claim amendments are presented, thus, no new matter is added.

In the Office Action, the drawings were objected to; Claims 21-28 were rejected under 35 U.S.C. §112, second paragraph; Claims 16 and 29 were rejected under 35 U.S.C. §102(e) as anticipated by Cusinato et al. (U.S. Patent No. 6,750,716, hereinafter Cusinato); and Claims 17-20 and 30 were objected to as dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Applicant appreciatively acknowledges the indication of allowable subject matter. However, since Applicant considers that independent Claim 16 patentably defines over the applied references, dependent Claims 17-20 and 30 are presently maintained in dependent form.

The outstanding Official Action objected to the drawings, and rejected Claims 21-28 under 35 U.S.C. §112, second paragraph, because various features recited in the claims were not depicted in the drawings. In response, new Figs. 10-19 are presented, which address the above noted objection to the drawings and rejection of the claims under 35 U.S.C. §112, second paragraph. Support for new Figs. 10-19 can be found at least at Figs. 4A-6 and pp. 12-17 of the originally filed specification.

More particularly, Figs 10 and 11 represent two embodiments of the invention with the polarized diode (transistor M4 in which gate and drain are connected together), and therefore illustrate two embodiments of Claim 19. Figs. 13-19 represent different embodiments of the invention wherein the amplifier comprises a slaving circuit, as recited in Claim 21. Figs. 12 and 13 illustrate two embodiments of the slaving circuit as "a resistor

connected between the drain of the first transistor and a fixed voltage," as recited in Claim 22. Figs. 14 and 15 illustrate two embodiments of the slaving circuit as "a read circuit in which the amplifier output voltage is applied to the input of said read circuit that forms the first and the second current generator" and wherein the amplifier comprises "a low pass filter by the read circuit," as recited in Claims 23 and 24. Figs. 16 and 17 illustrate two embodiments of the read circuit of Claim 23, wherein the read circuit "is a differential amplifier," as recited in Claim 26. Figs. 18 and 19 illustrate two embodiments of the slaving circuit as "a MOS transistor mounted with common gate to the amplifier output," as recited in Claim 28. Also, Claim 25 concerns the case in which the read circuit has a gain equal to 1 and, therefore, Claim 25 corresponds to figures 14 or 15 with the amplifier as having a gain equal to 1, and the features of Claim 27 are illustrated in Fig. 9.

Accordingly, in view of drawing amendments as discussed above, Applicant respectfully requests that the objection to the drawings, and the rejection of Claims 21-28 under 35 U.S.C. §112, second paragraph, be withdrawn.

In the outstanding Office Action, Claims 16 and 29 were rejected under 35 U.S.C. §102(e) as anticipated by Cusinato. Applicant respectfully traverses this rejection, as independent Claim 16 recites novel features clearly not taught or rendered obvious by the applied reference.

Independent Claim 16 recites a voltage amplifier comprising:

> a first field effect transistor with a gate, a drain, and a source, an amplifier input terminal being the gate of the first field effect transistor, and an amplifier output terminal being the drain of the first field effect transistor;
>
> a first current generator that charges the drain of the first transistor;
>
> a second current generator that charges the source of the first transistor, a value of the current output by the second current generator being substantially equal to a value of the current output by the first current generator;

a first capacitor with a first terminal connected to the drain of the first transistor and a second terminal connected to a first reference voltage;

a second capacitor with a first terminal connected to the source of the first transistor and a second terminal connected to a second reference voltage; and

an additional field effect transistor with a gate, a drain, and a source, of a type opposite to a type of the first field effect transistor, the drain of the additional transistor being connected to the drain of the first field effect transistor, the gate of the additional transistor being connected to a voltage that is or is not offset from the voltage applied to the gate of the first field effect transistor, the source of the additional field effect transistor being connected to the first current generator and to a first terminal of an additional capacitor, the second terminal of the additional capacitor being connected to a fixed voltage.

By way of the above noted configuration, the two current generators I1 and I0 of the voltage amplifier of the invention are identical and constant, and no signal modulation is introduced through the current generators. The current of the first current generator I1 accumulates on the additional capacitor C01. The current of the second current generator I0 (which may be seen as an electron constant flux Phi_e_0 (Phi_e_0 = -I0) going from the ground to the second capacitor C0) accumulates on the second capacitor C0.

At the same time, depending on the Vgs voltages of the first field effect transistor Ml and the additional field effect transistor M3, a current I_Madd is extracted from the additional capacitor C01 towards the output node through the additional field effect transistor M3, and a flux of electrons Phi_e_M1 is extracted from the second capacitor towards the output node through the first field effect transistor.

In a steady state:

$$I\_Madd = I1$$
$$Phi\_e\_Ml = Phi\_e\_0$$

Thus, in this case:

- Source voltages of Ml and M3 are stable; and

- I_Madd and Phi_e_M1 cancel at the output node, which voltage is stable.

If a modulation is introduced through the gate voltages of Ml and of the additional capacitor:

I1 and Phi_e_0 remain unchanged, and

currents through Ml and the additional MOSFET are transiently modified because the extraction of the stored charges from the second and additional capacitors are transiently modified. For example, if the input voltage increases, the electron flux through M1 increases and the corresponding electrons are extracted from the second capacitor, whose voltage increases, and at the same time the current through the additional MOSFET decreases and more positive charges are accumulated on the additional capacitor whose voltage also increases.

When a slaving circuit is used, the goal is to make the two current sources I0 and I1 identical, which otherwise is not practically feasible with two independent sources.

Turning to the applied reference, Cusinato describes a class AB operational amplifier having high gain and low setting time. In Cusinato's amplifier circuit, signal modulation is introduced through the gates of M10. Voltage modulation is converted to current modulation in the internal branches, and then copied on the external branches via the current mirrors 11, and signal modulation is introduced in the external branches through the top and bottom MOSFETs.

Thus, the gain stage 12, 13, 14 in Cusinato is not mandatory, even if welcome. As explained in the Bult reference mentioned in Cusinato, the goal of this gain stage is to fix the voltage of node 11b, to prevent any Vds modulation of the current mirror transistor when the output voltage varies, and prevent any decrease of the modulation injected by the current mirror when the output voltage varies. In other words, the gain stage increases the output impedance of the current mirror transistor.

In rejecting the features directed to the claimed first field effect transistor, the outstanding Office Action relies on the MOSFET 12 of Cusinato. However, the MOSFET 12 does not inject a signal modulation, but is used only to suppress a negative effect due to the poor output impedance of the current mirror transistor I1. Thus, MOSFET 12 of Cusinato can not reasonably be interpreted as the claimed "first field effect transitor," as recited in independent Claim 16.

The outstanding Office Action also cites the current mirror 11 of Cusinato in rejecting the claimed features directed to the claimed "first current generator." However, the current mirror transistor 11 of Cusinato injects the signal modulation in the external branch, so it cannot be seen as a constant current. The currents of the two mirrors (top and bottom) are identical only if the inputs of the differential amplifier (VI1 and VI2) are identical, and if VBl = VB2.

Further, the connection of the capacitor 14 to ground through resistor 25 cannot be seen as a connection to the ground, as asserted in the outstanding Office Action. A capacitor connected to ground via a resistor is almost ground, but this is true only in the case when the intermediate node voltage is almost equal to zero. In the case of Cusinato's circuit, the intermediate node 3a is the output of the amplifier, so the voltage of this node varies very much and cannot be considered as almost a ground (or constant voltage), as asserted in the outstanding Office Action.

Moreover, the connection of capacitor 14 to the source of MOSFET 12 via stage 13 cannot be similar to a direct connection, as asserted in the outstanding Office Action. In the case of Cusinato's circuit, the voltage of capacitor 14 modulates the gate voltage of transistor 12 (provided that the output impedance of amplifier 13 is not negligible), then the gate voltage variations modulate the source voltage of 11b of transistor 12, while amplifier 13

decreases the modulation on the gate of transistor 12. This is far from a direct connection. Moreover, only the voltage variations on capacitor 14 will finally affect the source voltage of transistor 12, but no charge can be extracted from capacitor 14 to flow through the channel of transistor 12 (which is biased in saturation mode). The operation of the claimed "second capacitor" is in clear contrast to the above noted description in Cusinato.

Similarly, in the upper branch, signal modulation is injected through the current mirror and MOSFET 12 is used merely to prevent a voltage modulation of node 11b.

Finally, Cusinato's schematics would not work if the gates of the upper and lower MOSFET 12 would be connected together, or identical. The circuit also would not function properly if the gate voltages would be offset one from the other. Thus, the gate voltages have to be defined from the top and bottom 11b node voltages, from DC and AC points of view. For example, if VI1 increases while VI2 remains constant, the current changes in the upper left transistor of the current mirror 11, while it remains constant in the lower left transistor of the current mirror 11. Then, the gate voltage of the top transistor 12 must be adapted while gate voltage of bottom transistor 12 must remain constant.

Therefore, for at least the reasons discussed above, Applicant respectfully submits Cusinato fails to teach or suggest various features recited in independent Claim 16. Accordingly, Applicant respectfully requests that the rejection of Claim 16 (and Claim 29, which depends therefrom) under 35 U.S.C. §102(e) be withdrawn.

Consequently, in view of the present amendment and in light of the foregoing comments, it is respectfully submitted that the invention defined by Claims 17-30 patentably define over the applied references. The present application is therefore believed to be in condition for formal allowance and an early and favorable reconsideration of the application is therefore requested.

Respectfully submitted,

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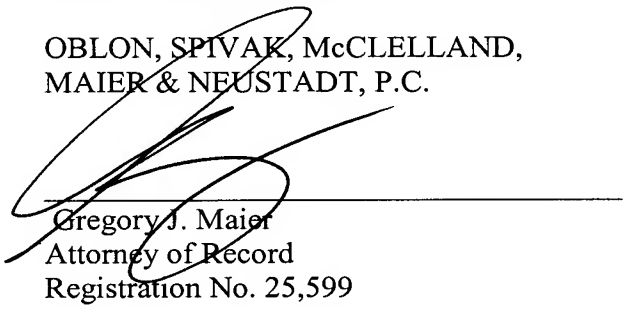

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